introducing into said crystal semiconductor a second impurity that gives one conductivity to form a source region and a drain region in said crystal semiconductor with said channel forming region therebetween,

wherein a carrier moves through said intrinsic or substantially intrinsic region while said carrier avoids said impurity region formed in said part to become the channel forming region.

3. (Amended) A method of manufacturing an insulated gate semiconductor device, said method comprising the steps of:

locally conducting an anisotropic etching on a surface of a substrate comprising silicon to draw a groove-like or hole-like pattern in a part of said substrate to become a channel forming region:

adding said surface of said substrate with an impurity selected from the group consisting of carbon, nitrogen and oxygen;

embedding said groove-like or hole-like pattern with thermal oxide by conducting a heat treatment on said substrate after the adding step to make said impurity segregated in said thermal oxide.

5. (Amended) A method of manufacturing an insulated gate semiconductor device, said method comprising the steps of:

locally conducting an anisotropic etching on a surface of a substrate comprising silicon and containing boron to draw a groove-like or hole-like pattern in a part of said substrate to become a channel forming region;

adding said surface of said substrate with an impurity selected from the group consisting of carbon, nitrogen and oxygen;

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embedding said groove-like or hole-like pattern with thermal oxide by conducting a heat treatment on said substrate after the adding step to make said impurity segregated in said thermal oxide and to make said boron segregated in said thermal oxide.

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7. (Amended) A method of manufacturing an insulated gate semiconductor device, said method comprising the steps of:

implanting an oxygen ion into a crystal semiconductor comprising a part to become a channel forming region by a convergent ion beam or an electron beam, said crystal semiconductor comprising silicon;

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forming an intrinsic or substantially intrinsic region and an oxide region in said part to become the channel forming region by thermally treating said crystal semiconductor comprising silicon to change a region of said crystal semiconductor implanted with said oxygen ion by said implanting step into said oxide region; and

introducing into said crystal semiconductor an impurity that gives one conductivity to form a source region and a drain region in said crystal semiconductor with said channel forming region therebetween,

wherein a carrier moves through said intrinsic or substantially intrinsic region while said carrier avoids said oxide region formed in said part to become the channel forming region.

Sub C3

9. (Amended) A method of manufacturing an insulated gate semiconductor device, said method comprising the steps of:

forming an intrinsic or substantially intrinsic region and an impurity region in a part of a crystal semiconductor to become a channel forming region by introducing a first impurity into said impurity region, said impurity region containing an element selected from the group consisting of carbon, nitrogen and oxygen as said first impurity; and

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introducing into said crystal semiconductor a second impurity that gives one conductivity to form a source region and a drain region in said crystal semiconductor with said channel forming region therebetween,

wherein a carrier moves through said intrinsic or substantially intrinsic region while said carrier avoids said impurity region formed in said part to become the channel forming region.

Sub D1

11. (Amended) A method of manufacturing an insulated gate semiconductor device, said method comprising the steps of:

locally conducting an anisotropic etching on a surface of a substrate comprising silicon to draw a groove-like or hole-like pattern in a part of said substrate to become a channel forming region;

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adding said surface of said substrate with an impurity selected from the group consisting of carbon, nitrogen and oxygen;

embedding said groove-like or hole-like pattern with thermal oxide by conducting a heat treatment on said substrate after the adding step to make said impurity segregated in said thermal oxide,

wherein said impurity is added by said adding step to said substrate to a depth deeper than an etched depth formed in said groove-like or hole-like pattern by said anisotropic etching.

13. (Amended) A method of manufacturing an insulated gate semiconductor device, said method comprising the steps of:

forming an intrinsic or substantially intrinsic region and a plurality of impurity regions in a part of a crystal semiconductor to become a channel forming region by introducing a first impurity into said impurity regions, said plurality of impurity regions containing an element selected from the group consisting of carbon, nitrogen and oxygen as said first impurity;

introducing into said crystal semiconductor a second impurity that gives one conductivity to form a source region and a drain region in said crystal semiconductor with said channel forming region therebetween,

wherein said impurity regions alternate with said intrinsic or substantially intrinsic region in a direction of a channel width W of said channel forming region, and

wherein said impurity regions have total width of Wpi in a direction of said channel width W, and a total width of said intrinsic or substantially intrinsic region is Wpa in said direction of said channel width W, where Wpi/W = 0.1 to 0.9 and Wpa/W = 0.1 to 0.9.

15. (Amended) A method of manufacturing an insulated gate semiconductor device, said method comprising the steps of:

forming a resist over a crystal semiconductor comprising a part to become a channel forming region;

forming a dotted hole in said resist by patterning said resist using electron drawing method or FIB method;

forming an intrinsic or substantially intrinsic region and a plurality of impurity regions in said part to become the channel forming region by introducing a first impurity into said impurity regions through said resist having said dotted hole, said first impurity being selected from the group consisting of carbon, nitrogen and oxygen; and

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introducing into said crystal semiconductor a second impurity that gives one conductivity to form a source region and a drain region in said crystal semiconductor with said channel forming region therebetween,

wherein said impurity regions form one or a plurality of rows extending in a direction of a channel length of said channel forming region, and

wherein a carrier moves through said intrinsic or substantially intrinsic region while said carrier avoids said impurity regions formed in said part to become the channel forming region.

Sub D1

17. (Amended) A method of manufacturing an insulated gate semiconductor device, said method comprising the steps of:

locally conducting an anisotropic etching on a surface of a substrate comprising silicon to draw a groove-like or hole-like pattern in a part of said substrate to become a channel forming region;

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adding said surface of said substrate with an impurity selected from the group consisting of carbon, nitrogen and oxygen;

embedding said groove-like or hole-like pattern with thermal oxide by conducting a heat treatment on said substrate

after the adding step to make said impurity segregated in said thermal oxide,

wherein said impurity segregated in said thermal oxide forms a plurality of impurity regions

wherein said impurity regions form one or a plurality of rows extending in a direction of a channel length of said channel forming region.

18. (Amended) A method of manufacturing an insulated gate semiconductor device, said method comprising the steps of:

forming a source region, a drain region and a channel forming region using a crystal semiconductor;

forming an intrinsic or substantially intrinsic region and an impurity region in said channel forming region; and

forming a gate insulating film and a gate electrode over said channel forming region,

wherein said impurity region formed in said channel forming region pins a depletion layer that expands from said drain region toward said channel forming region and said source region, and

wherein a carrier moves through said intrinsic or substantially intrinsic region while said carrier avoids said impurity region formed in said channel forming region.

19. (Amended) A method of manufacturing an insulated gate semiconductor device, said method comprising the steps of:

forming a source region, a drain region and a channel forming region using a crystal semiconductor;

forming an intrinsic or substantially intrinsic region and an impurity region in said channel forming region;

forming a gate insulating film and a gate electrode over said channel forming region,

wherein said impurity region controls the threshold voltage to a predetermined value voltage, and

wherein a carrier moves through said intrinsic or substantially intrinsic region while said carrier avoids said impurity region formed in said channel forming region.

Sub C5

20. (Amended) A method of manufacturing an insulated gate semiconductor device, said method comprising the steps of:

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forming a source region, a drain region and a channel forming region using a crystal semiconductor;

forming an intrinsic or substantially intrinsic region and an impurity region in said channel forming region; and

forming a gate insulating film and a gate electrode over said channel forming region,

wherein an impurity element that expand an energy band width (Eg) is added to said impurity region, and

wherein a carrier moves through said intrinsic or substantially intrinsic region while said carrier avoids said impurity region formed in said channel forming region.

Sub D7

21. (Amended) A method of manufacturing an insulated gate semiconductor device, said method comprising the steps of:

forming a source region, a drain region and a channel forming region using a crystal semiconductor;

forming an intrinsic or substantially intrinsic region and an impurity region in said channel forming region; and

forming a gate insulating film and a gate electrode over said channel forming region,

wherein said impurity region pins a depletion layer that expands from said drain region toward said channel forming region and said source region,

wherein an impurity element that expands an energy band width (Eg) is added to said impurity region, and

wherein a carrier moves through said intrinsic or substantially intrinsic region while said carrier avoids said impurity region formed in said channel forming region.

22. (Amended) A method of manufacturing an insulated gate semiconductor device, said method comprising the steps of:

forming a source region, a drain region and a channel forming region using a crystal semiconductor;

forming an intrinsic or substantially intrinsic region and an impurity region in said channel forming region; and

forming a gate insulating film and a gate electrode over said channel forming region,

wherein said impurity region controls the threshold voltage to a predetermined value voltage,

wherein an impurity element that expand an energy band width (Eg) is added to said impurity region, and

wherein a carrier moves through said intrinsic or substantially intrinsic region while said carrier avoids said impurity region formed in said channel forming region.

23. (Amended) A method of manufacturing an insulated gate semiconductor device, said method comprising the steps of:

forming a source region, a drain region and a channel forming region using a crystal semiconductor; and

forming an intrinsic or substantially intrinsic region and an impurity region in said channel forming region; and

forming a gate insulating film and a gate electrode over said channel forming region,

wherein said impurity region has an insulating property,

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wherein an impurity element that expands an energy band width (Eg) is added to said impurity region, and

wherein a carrier moves through said intrinsic or substantially intrinsic region while said carrier avoids said impurity region formed in said channel forming region.

SUB D1

66. (Amended) A method of manufacturing an insulated gate semiconductor device, said method comprising the steps of:

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locally conducting an anisotropic etching on a surface of a substrate comprising silicon and containing boron to draw a groove-like or hole-like pattern in a part of said substrate to become a channel forming region;

adding said surface of said substrate with an impurity selected from the group consisting of carbon, nitrogen and oxygen;

embedding said groove-like or hole-like pattern with thermal oxide by conducting a heat treatment on said substrate after the adding step to make said impurity segregated in said thermal oxide and to make said boron segregated in said thermal oxide,

wherein said impurity segregated in said thermal oxide forms a plurality of impurity regions

wherein said impurity regions form one or a plurality of rows extending in a direction of a channel length of said channel forming region.

Please add claims 68-73.

- -68. (New) A method according to claim 1 wherein said intrinsic or substantially intrinsic region contains phosphorus or boron, and concentration of phosphorus or boron therein is 5 x 10^{17} atoms/cm^3 or less, and said intrinsic or substantially intrinsic region contains carbon, nitrogen or oxygen, and concentration of carbon, nitrogen or oxygen therein is 2 x 10^{18} atoms/cm^3 or less.

69. (New) A method according to claim 7 wherein said intrinsic or substantially intrinsic region contains phosphorus or boron, and concentration of phosphorus or boron therein is 5 x 10^{17} atoms/cm^3 or less, and said intrinsic or substantially intrinsic region contains carbon, nitrogen or oxygen, and concentration of carbon, nitrogen or oxygen therein is 2 x 10^{18} atoms/cm^3 or less.

70. (New) A method according to claim 9 wherein said intrinsic or substantially intrinsic region contains phosphorus or boron, and concentration of phosphorus or boron therein is 5 x 10^{17} atoms/cm^3 or less, and said intrinsic or substantially intrinsic region contains carbon, nitrogen or oxygen, and concentration of carbon, nitrogen or oxygen therein is 2 x 10^{18} atoms/cm^3 or less.

71. (New) A method according to claim 13 wherein said intrinsic or substantially intrinsic region contains phosphorus or boron, and concentration of phosphorus or boron therein is 5 x 10^{17} atoms/cm^3 or less, and said intrinsic or substantially intrinsic region contains carbon, nitrogen or oxygen, and

concentration of carbon, nitrogen or oxygen therein is 2 x 10^{18} atoms/cm^3 or less.

SUB D1

72. (New) A method according to claim 15 wherein said intrinsic or substantially intrinsic region contains phosphorus or boron, and concentration of phosphorus or boron therein is 5 x 10^{17} atoms/cm^3 or less, and said intrinsic or substantially intrinsic region contains carbon, nitrogen or oxygen, and concentration of carbon, nitrogen or oxygen therein is 2 x 10^{18} atoms/cm^3 or less.

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73. (New) A method according to claim 18 wherein said intrinsic or substantially intrinsic region contains phosphorus or boron, and concentration of phosphorus or boron therein is 5 x 10^{17} atoms/cm^3 or less, and said intrinsic or substantially intrinsic region contains carbon, nitrogen or oxygen, and concentration of carbon, nitrogen or oxygen therein is 2 x 10^{18} atoms/cm^3 or less. - -